## IN THE ABSTRACT

*Please replace the abstract with the following new abstract. The abstract is also submitted on a separate sheet with the response.*

A memory device includes a cell area having N+1 unit cell blocks. Each cell block includes M word lines. The N unit cell blocks are each corresponded to a logical cell block address. The one additional unit cell block is added for accessing data with high speed. A tag block receives a row address, senses the logical cell block address in the row address and outputs a physical cell block address based on the logical cell block address and the candidate information. The tag block includes:N+1 unit tag tables corresponding to the N+1 unit cell blocks. Each tag block has M number of registers. The M number of registers correspond to M number of word lines of the corresponding unit cell blocks. Each register stores one logical cell block address. The tag block also includes an initialization unit that initializes the N+1 unit tag tables.

## IN THE DESCRIPTION

*Please amend the paragraph beginning on page 9 line 27 as follows:*

In accordance with an aspect of the present invention, there is provided a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines; a predetermined cell block table for storing a-candidate information representing at least more than one candidate word line among the M number of the-word lines to be-stored data; and a tag block for receiving a row address, sensing a logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information, wherein the tag block includes: a N+1 number of unit tag tables, each having M number of registers and storing a store information that the registers correspondscorrespond to M number of word lines, each register storingstores each the physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information; and an initialization unit for initializing the N+1 number of unit tag tables.

## ABSTRACT

A memory device includes a cell area having N+1 unit cell blocks. Each cell block includes M word lines. The N unit cell blocks are each corresponded to a logical cell block address. The one additional unit cell block is added for accessing data with high speed. A tag block receives a row address, senses the logical cell block address in the row address and outputs a physical cell block address based on the logical cell block address and the candidate information. The tag block includes:N+1 unit tag tables corresponding to the N+1 unit cell blocks. Each tag block has M number of registers. The M number of registers correspond to M number of word lines of the corresponding unit cell blocks. Each register stores one logical cell block address. The tag block also includes an initialization unit that initializes the N+1 unit tag tables.